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10/759,915	01/16/2004	Yan Chong	174/305	8041

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EXAMINER

LE, DINH THANH

ART UNIT PAPER NUMBER

2816

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/759,915

Applicant(s)

CHONG ET AL

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

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## **DETAILED ACTION**

### ***Drawings***

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections***

#### ***Claim Rejections - 35 USC § 112***

Claims 1- 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, it is unclear what the "particular net number" on line 8 is. The same is true for claims 32 and 36.

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In claim 8, the description of the present invention is incomplete because the programmable logic circuit is not connected to anything. Thus, the claimed logic circuit may not perform the recited function.

In claims 10, 33 and 38, it is unclear what the “user inputs” are and how they are read on the preferred embodiment or seen on the drawings. The same is true for reciting “bandwidth control signal is provided by RAM bits” in claims 11, 34 and 39, “oscillator” in claim 20, “clock signal distribution circuitry” on line 5 of claim 22.

In claims 12, 35 and 40, it is unclear how the bandwidth control signal can be adjustable during operation since no means for performing adjusting function is recited in this claim. The same is true for reciting “reset level is adjustable during operation” in claims 18,

In claim 23, the recitation “said input clock signal” on line 4 lacks antecedent basis. it is not understood where the input clock signal comes from, what the “regions” on line 3 are, how the regions can use the input clock signal. Also, the recitation “a programmable logic device” on line 5 is confusing because it is unclear if this is an additional “logic device” or a further recitation of the previously claimed “logic device” on line 1 of claim 21. The same is true for claim 24, and for reciting “an integrated circuit” on line 5 of claim 28-29.

In claim 32, it is unclear how the internal clock signal can be “adjusted” on line 9, and how the bandwidth control signal can control the particular net number since no means for performing the adjusting function is recited in the claim

The remaining claims are dependent from the above claims and therefore also considered indefinite.

***Claim Rejections - 35 USC § 102***

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 19-22, 27 and 36 are rejected under 35 USC 102 (b) as being anticipated by Saitoh et al (US 5,604,775).

Saitoh et al disclose a DLL circuit in Figure 3 comprising:

- a phase comparator (30) for comparing a feedback signal derived from said internal clock signal with said reference clock signal;
- a setting counter or a low pass filter circuitry (40) that is adjusted by said phase comparator (30) after a particular net number of either lead or lag comparisons by said phase comparator (30);
- a compensation component (10) for receiving said reference clock signal and, based on said setting counter (40), producing said internal clock signal;
- wherein said feedback signal is substantially the same signal as said internal clock signal or a delayed version of said internal feedback signal clock signal;
- wherein said reference clock signal is a clock signal from an inherent circuitry external to said loop circuit. reference clock, i.e., an oscillator since the reference clock signal is an oscillating signal as recited in claim 4-5; and
- wherein said phase comparator for comprises a phase detector 30) for producing lead or lag between said feedback signal and said reference signal

With regard to claim 19-20, the compensation component comprises a delay line (11, 12) for producing said internal clock controlled delay signal, noted that the delay line is interpreted as a controlled oscillator because it produces oscillating internal clock signal. loop

With regard to claim 23, the reciting "clock signal distribution circuitry" is read on element (20 of Saitoh et al and the regions are interpreted as areas outside the element (20).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23-26 and 28-31 are rejected under 35 USC 103 (a) as being unpatentable over Sung et al (6,437,650) in view of Saitoh et al (US 5,604,775)).

Sung et al discloses in Figure 5 a circuit comprising:

- a processing circuitry (204);
- a memory (206); and
- a programmable logic device (10) coupled to the processing circuitry (204) and the memory (206).

However, Sung et al does not disclose that the programmable logic device comprises the combination of the phase comparator, the setting counter and the compensating component as recited in claim 1. Saitoh et al discloses in Figure 3 a DLL circuit with all of the limitations of claim 1 as stated above for reducing phase jitter, see lines 30-33, column 1. It would have been

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obvious to a person having skill in the art at the time the invention was made to employ the DLL circuit taught by Saitoh et al in the circuit of Sung et al for the purpose of reducing phase jitter.

With regard to claims 25-26 and 29-31, although Sung et al does not disclose that the processing

circuitry, a memory and the logic device are mounted on a printed circuit board; however, as well known in the art, all of components (204, 206, 10) as shown in Figure 5 of Sung et al are the integrated circuits so that they can be mounted on a printed circuit board for reducing size.

Therefore, mounting all of the components (10, 204, 206) for the purpose of reducing size is considered to be a design expedient for an engineer depending upon a particular application in which the modified circuit of Sung et al is to be used that would have been obvious at the time of the invention.

#### ***Allowable Subject Matter***

Claims 32-35 are allowed.

Claims 8-18 and 37-40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claims are allowable because the prior art of record does not show the programmable logic circuit for adjusting the counter as combined in claim 8 and the particular net number is controlled by a bandwidth control signal as combined in claim 32.

#### ***Conclusion***

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Dinh Le', with a long horizontal flourish extending to the right.

DINH LE  
Primary Examiner